AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1-23. (Cancelled)

24. (Currently amended) A method comprising:

transferring read data from a first agent, the first agent being coupled to a half-duplex bus;

issuing a preempt signal from a second agent, the second agent being coupled to the half-duplex bus;

determining whether to allow preemption of the read data based at least in part on an amount of pending read requests for the first agent; and

if preemption is allowed:

determining a suitable point to preempt the read data transfer;

temporarily halting the read data transfer,

transferring a read data request from the second agent to the first agent, and

resuming the read data transfer.

25. (Previously Presented) The method of claim 24, wherein the first agent comprises a memory controller.

26. (Previously Presented) The method of claim 25, wherein the second agent comprises an input/output device.

27. (Previously Presented) The method of claim 24, wherein determining whether to allow preemption of the read data comprises determining if pending read requests for the second agent are below a threshold.

28. (Previously Presented) The method of claim 24, wherein determining a suitable point to preempt the read data transfer comprises identifying a cacheline boundary.

29. (Previously Presented) The method of claim 24, further comprising allowing transfer of a limited number of read requests before resuming the read data transfer.

30. (Previously Presented) A method comprising:

transferring read data over a half-duplex bus from a memory controller;

issuing a first signal indicating that an I/O device has a read request pending;

issuing a second signal requesting preemption of the transfer of read data;

if a number of read requests held by the memory controller is below a threshold:

electing a suitable point for preemption of the transfer of read data,

pausing transmission of read data;

providing control of the half-duplex bus to the I/O device,

transferring the read request from the I/O device to the memory controller over the half-duplex bus,

providing control of the half-duplex bus to the memory controller, and

resuming transfer of read data.

31. (Previously Presented) The method of claim 30, further comprising sampling the first signal and the second signal.

32. (Previously Presented) The method f claim 30, wherein the thresh ld is an indicator of imminent read starvation.

33. (Previously Presented) The method of claim 30, wherein the suitable point for preemption of the transfer of read data comprises a cacheline boundary.

34. (Previously Presented) The method of claim 30, wherein a transition period from pausing transfer of read data to transferring the read request is one clock period.

35. (Previously Presented) The method of claim 34, wherein a transition period from transferring the read request to resuming transfer of the read data is one clock period.

36. (Previously Presented) The method of claim 30, wherein the memory controller includes an arbiter that executes an arbitration protocol.

37. (Previously Presented) The method of claim 30, wherein the arbiter of the memory controller executes a preemption algorithm to elect the suitable point for preemption.

38. (Presently Presented) A computer system comprising:

a half duplex bus;

a first agent and a second agent, the first agent and the second agent each being coupled to the half-duplex bus, the first agent and the second agent each comprising an arbiter that follows an algorithm to determine ownership of the half-duplex bus;

a request line coupled between the first and second agents, the request line being asserted by the second agent to request ownership of the half-duplex bus from the first agent; and

a preempt line, a preempt signal being asserted by the second agent on the preempt line to request temporary preempti n of data transfer by the first agent to allow transmission of a read request, the first agent to allow preemption if a number of pending read requests for the first agent is less than a threshold, the first agent to determine a suitable point for preemption of data transfer.

39. (Previously Presented) The computer system of claim 38, wherein the second agent asserts the preempt signal during a current read return from the first agent.

40. (Previously Presented) The computer system of claim 38, wherein the suitable point comprises a cacheline boundary.

41. (Previously Presented) The computer system of claim 38, wherein the first agent comprises a memory controller.

42. (Previously Presented) The computer system of claim 41, wherein the second agent comprises an input/output (I/O) device.

43. (Currently amended) A computer system comprising:

means for transferring read data by a first agent, the first agent being coupled to a half-duplex bus;

means for transferring a preemption signal from a second agent to the first agent, the second agent being coupled to the half-duplex bus;

means for determining whether to grant preemption based on an amount of pending read requests for the first agent;

means for determining an appropriate point for preemption;

means for temporarily suspending the transference of read data in response to the preemption signal;

means for transferring a read request from the second agent to the first agent after suspension of the transference of read data; and

means for resuming transference of read data after transference of the read request.

44. (Previously Presented) The computer system of claim 43, wherein the first agent comprises a memory controller.

45. (Previously Presented) The computer system of claim 43, wherein the second agent comprises an input/output device.

46. (Presently Presented) The computer system of claim 43, wherein the means for determining whether to grant preemption comprises means for determining whether pending read requests for the first agent are below a threshold.

47. (Previously Presented) The computer system of claim 43, wherein means for determining an appropriate point for preemption comprise means for identifying a cacheline boundary.